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EXAMINER	
CHRZANOWSKI, MATTHEW R	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,394	SIEGELIN ET AL.	
	Examiner	Art Unit	
	Matthew R. Chrzanowski	2198	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27 and 29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/22/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Multiple dependent **claim 28** improperly depends on another multiple dependent **claim 26**. Therefore **claim 28** is withdrawn from consideration.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 1-27, and 29-31** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

5. **Claims 1 and 13** recites the limitation "**the same logical area**" in page 3, line 4 of claim 1 and page 5, line 7 of claim 13. There is insufficient antecedent basis for this limitation in the claim.

6. **Claims 1 and 13** recites the limitation "**the content**" in page 3, line 5 of claim 1 and page 5, line 8 of claim 13. There is insufficient antecedent basis for this limitation in the claim.

7. **Claims 1 and 13** recites the limitation "**said logical area**" in page 3, lines 4 and 5 of claim 1; page 5, line 7 and 8 of claim 13. There is insufficient antecedent basis for this limitation in the claim.

8. **Claims 1 and 13** recites the limitation "**said blank mirror areas**" in page 3, line 5 of claim 1 and page 5, lines 8-9 of claim 13. There is insufficient antecedent basis for this limitation in the claim.

9. **Claims 1 and 13** recites the limitation "**the active area**" in page 3, line 6 of claim 1 and page 5, line 9 of claim 13. There is insufficient antecedent basis for this limitation in the claim.

10. **Claim 4** recites the limitation "**the active physical area**" in page 3, line 2 of claim 4. There is insufficient antecedent basis for this limitation in the claim.

11. **Claim 4** recites the limitation "**the first area**" in page 3, line 4 of claim 4. There is insufficient antecedent basis for this limitation in the claim.

12. **Claim 5** recites the limitation "**the erasure**" in page 3, line 2 of claim 5. There is insufficient antecedent basis for this limitation in the claim. There is no prior reference to an erasure in claim 1.

13. **Claim 5** recites the limitation "**the system**" in page 3, line 3 of claim 5. There is insufficient antecedent basis for this limitation in the claim.

14. **Claim 7** recites the limitation "**said active physical areas**" in page 4, line 3 of claim 7. There is insufficient antecedent basis for this limitation in the claim.

15. **Claim 8** recites the limitation "**said logical area**" in page 4, line 4 of claim 8. There is insufficient antecedent basis for this limitation in the claim. There are multiple logical areas claimed, one in claim 1 and one in 8.

16. **Claim 11** recites the limitation "**the blank mirror area**" in page 4, lines 5-6 of claim 11. There is insufficient antecedent basis for this limitation in the claim.

17. **Claim 12** recites the limitation "**the blank mirror area**" in page 4, line 6 of claim 12. There is insufficient antecedent basis for this limitation in the claim.

18. **Claims 2-3, 6, 9-10, and 14-27, 29-31** inherit the above stated defects.

Claim Rejections - 35 USC § 102

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

20. **Claims 1-2, 11, 13, and 23** are rejected under 35 U.S.C. 102(b) as being anticipated by **Ban (WO 94/20906 hereinafter "Ban")**.

Consider **claims 1 and 13**, Ban discloses a method to write in flash type memory *(flash memory, abstract; method (i.e., software, or firmware of hardware)..., page 2, lines 7-10)* of an electronic module comprising associating at least two physical areas of said memory *(flash memory physical address locations, page 2, line 21)*, called mirror areas, with the same logical area *(fixed-*

length group of physical byte addresses form a logical block, page 3, lines 1-2; one or more physically contiguous flash memory areas or zones comprise a number of blocks, page 3, lines 4-7; therefore the physical byte addresses are associated with logical blocks, zones and units, FIG. 2, 3, & 7) and during a write *(abstract)* in said logical area, in programming the content of said logical area in one of said blank mirror areas, called the active area *(flash memory system which "allows data to be continuously written to unwritten physical address locations," abstract; data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29) (page 7, lines 1 - page 9, line 22 and page 13, claim 1).*

Consider **claims 2 and 23**, and as applied to **claims 1 and 13** above, Ban discloses the method comprising erasing the content of all mirror areas used in a single operation at a convenient time *("One or more physically contiguous flash memory areas (called zones) that can be physically erased using suitable prior art flash memory technology comprise a unit and each unit contains an integral number of blocks," page 3, lines 4-7; there is a zone erase operation that erases the unit that includes that block, and unit containing the logical block consisting of multiple physical address locations are therefore all erased, the page 3, lines 24-25) (page 7, lines 1 - page 9, line 22 and page 13, claim 1).*

Consider **claim 11**, Ban discloses an electronic module having information processing means *(the device writes and stores data, abstract)* and comprising a flash type non volatile memory *(flash memory, abstract)* having a mirror memory formed from at least two physical areas *(flash memory physical address locations, page 2, line 21)* and associated with the same logical area *(fixed-length group of physical byte addresses form a logical block, page 3, lines 1-2; one or more physically contiguous flash memory areas or zones comprise a number of blocks, page 3, lines 4-7; therefore the physical byte addresses are associated with logical blocks, zones and units, FIG. 2, 3, & 7)*, each new programming operation in said logical area taking place in an area of the blank mirror area*(flash memory system which "allows data to be continuously written to unwritten physical address locations," abstract; data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29) (page 7, lines 1 - page 9, line 22 and page 13, claim 1).*

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

23. **Claims 3, 7-8, 18, 24, and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** as applied to **claims 1-2, 13, and 23** above, and further in view of **Assar et al. (WO 95/10083 hereinafter "Assar").**

Consider **claims 3 and 24**, and as applied to **claims 2 and 23** above, Ban discloses the method comprising performing an erasure as described above in claim 2 and 23.

However, Ban does not disclose the method comprising performing the erasure during a period of inactivity or when all the mirror physical areas are used.

Assar discloses a method comprising performing an erasure when all the mirror physical areas are used *(when physical memory is filled, blocks with certain flags set are erased, wherein as described above blocks contain multiple physical mirror areas, page 20, lines 10-19)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform an erasure when all the mirror

physical areas are used in the system of Ban, because Assar teaches it is necessary to erase some data when a memory is full in order to place new data in a flash memory *(page 20, lines 10-19)*.

Consider **claims 7**, and as applied to **claims 1** above, Ban discloses the method comprising designating said active physical areas *(active unit made up of active blocks, FIG. 7; page 9, lines 27-30; page 10, line 1)*.

However, Ban does not disclose the method comprising designating said active physical areas using a counter incremented on each change of active area.

Assar discloses a method comprising designating active physical areas using a counter *(counter 620 page 18, lines26-page 19, line 1; page 20, line 17 and 26; counter 620 is used in conjunction with flags such as the used/free flag 112)* incremented on each change of active area *(page 20, lines 10-19)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to designate active physical areas using a counter in the system of Ban, because Assar teaches a counter is used to show the number of times a block has been erased and written (which areas are most and least worn out) in order to determine where to write next *(page 18, lines 26-28; abstract)*.

Consider **claims 8 and 29**, and as applied to **claims 1 and 13** above, Ban discloses the method of claims 1 and 13.

However, Ban does not disclose the method comprising associating at least one bit with a logical area representing the use state of at least one mirror physical area of said logical area.

Assar discloses a method comprising associating at least one bit *(one bit used flag 626, page 18, line 36)* with a logical area *(data block, page 18, lines 31-37)* representing the use state of at least one mirror physical area of said logical area *(page 18, lines 35-37)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate at least one bit with a logical area representing the use state of at least one mirror physical area of said logical area in the system of Ban, because Assar teaches used/free flag is used to avoid an erase-before-write cycle and therefore avoid the overhead of an erase cycle *(page 7, lines 9-21)*.

Consider **claim 18**, and as applied to **claim 7** above, Ban in view of Assar discloses the method of claim 7.

However, Ban does not disclose the method comprising associating at least one bit with a logical area representing the use state of at least one mirror physical area of said logical area.

Assar discloses a method comprising associating at least one bit *(one bit used flag 626, page 18, line 36)* with a logical area *(data block, page 18, lines 31-37)* representing the use state of at least one mirror physical area of said logical area *(page 18, lines 35-37)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate at least one bit with a logical area representing the use state of at least one mirror physical area of said logical area in the system of Ban, because Assar teaches used/free flag is used to avoid an erase-before-write cycle and therefore avoid the overhead of an erase cycle *(page 7, lines 9-21)*.

24. **Claims 4 and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** as applied to **claims 1 and 13** above, and further in view of **Mennecart (WO 01/88926 A1 hereinafter "Mennecart").**

Consider **claims 4 and 25**, and as applied to **claims 1 and 13** above, Ban discloses the method of claims 1 and 13.

However Ban does not disclose the method comprising copying the active physical area into a buffer area, erasing all mirror physical areas and copying the buffer into the first area available.

Mennecart discloses method comprising copying the active physical area into a buffer area *(buffer, abstract; step F5, temporary storage, FIG. 4)*, erasing

all mirror physical areas *(steps F3 and F3', FIG. 4)* and copying the buffer into the first area available *(page 5, line 1 – page 6, line 22; step F7, FIG. 4)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to copy the active physical area into a buffer area, erase all mirror physical areas and copy the buffer into the first area available in the system of Ban, because Mennecart teaches the method to process a write command in memory such as EEPROM, a type of flash memory in smart cards, which reduces the time required for processing *(page 3, lines 9-35; abstract)*.

25. **Claims 5 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** as applied to claim **claims 1-2 and 13** above, and further in view of **Hazen et al. (WO 99/35650 hereinafter "Hazen").**

Consider **claims 5 and 26**, and as applied to **claims 1-2 and 13** above, Ban discloses the method comprising performing an erasure as described in **claims 2 and 13**.

However, Ban does not disclose the method comprising the erasure and programming/read operations in parallel without blocking the system.

Hazen discloses a method comprising programming/read operations in parallel without blocking a system *("read-while-write operations," title; abstract; page 2, paragraph 4; pages 5-7)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use programming/read operations in parallel with erasure without blocking a system in the system of Ban, because Hazen teaches simultaneous operations is desired and an advantage in a flash memory device in terms of time constraints *(page 2, paragraph 2 and page 3, paragraph 1)*.

26. **Claims 6 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** in view of **Hazen et al. (WO 99/35650 hereinafter "Hazen")** as applied to **claims 5 and 26** above, and in view of **Lipovski (US Patent # 5758148)**.

Consider **claims 6 and 27**, and as applied to **claims 5 and 26** above, Ban in view of Hazen discloses the method wherein comprises performing the erasure and programming/read operations in parallel, having mirror area(s), one area being used for programming/reading while the other area is erased as described above in claims 5 and 26.

However, Ban does not disclose the method wherein comprises performing the erasure and programming/read operations in parallel **in a bi-bank memory**, each bank having mirror area(s), one bank being used for programming/reading while the other bank is erased, **the method changing**

active bank when all mirror areas of the bank used for programming/read have been used.

Hazen discloses the method wherein comprises performing the erasure and programming/read operations in parallel *(one device may be written to, while the other device is being erased, page 2, paragraph 3)* in a bi-bank memory *(multiple flash memory devices, page 2, paragraph 3)*, each bank having mirror areas *(as described in claims 5 and 26)*, one bank being used for programming/reading while the other bank is erased *(one device may be written to, while the other device is being erased, page 2, paragraph 3)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use programming/read operations in parallel in a bi-bank memory in the system of Ban, because Hazen teaches simultaneous operations is desired and an advantage in a flash memory device in term of time constraints *(page 2, paragraph 2; and page 3, paragraph 1)*.

Lipovski discloses a method of changing an active bank when all areas of the bank used for programming/read have been used *(one memory bank reaches its capacity, the system switches to the other bank to permit data writes, column 11, lines 38-42)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to change the active bank when all areas of the active bank have been used for programming operations in the system of

Ban, because Lipovski teaches this allows to continue writing to memory without erasing the full memory bank *(column 11, lines 38-42)*.

27. **Claims 9-10 and 30-31** rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** as applied to **claims 1-2 and 13** above, and further in view of **Kuo (US Patent # 4763305 hereinafter "Kuo").**

Consider **claims 9 and 30**, and as applied to **claims 1 and 13** above, Ban discloses wherein the write is carried out as claims 1 and 13 above.

However, Ban does not disclose the method, wherein the write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank physical area otherwise.

Kuo discloses a method, wherein a write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area *(if data in the area is the same as the data to be written, then avoid the erase/program cycle the data and the write is complete for that area, column 6, lines 18-26)*, and in a blank physical area otherwise *(if old data in byte or block is already in erased state or blank, or the data does not match so the physical area is erased or blank and then the write is performed; column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include when the write is carried out in

an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank physical area otherwise, in the system of Ban, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

Consider **claims 10 and 31**, and as applied to **claims 9 and 13** above, Ban discloses the method comprising programming *(writing)* of the logical area in the blank physical area in claim 1 and 13.

However, Ban does not disclose the method comprising programming only part of the logical area in the blank physical area.

Kuo discloses a method comprising programming only part of the logical area in the blank physical area *(only erase/program those areas which need to be, those areas that new data is same as old do not need to be erased and subsequently reprogrammed, column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to be able to program only part of the logical area in the blank physical area in the system of Ban, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

28. **Claim 12** rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** and further in view of **Robinson et al. (US Patent # 5375222).**

Consider **claim 12**, Ban discloses an electronic module having information processing means *(the device writes and stores data, abstract)* and comprising a flash type non volatile memory *(flash memory, abstract)* having a mirror memory formed from at least two physical areas *(flash memory physical address locations, page 2, line 21)* and associated with the same logical area *(fixed-length group of physical byte addresses form a logical block, page 3, lines 1-2; one or more physically contiguous flash memory areas or zones comprise a number of blocks, page 3, lines 4-7; therefore the physical byte addresses are associated with logical blocks, zones and units, FIG. 2, 3, & 7)*, each new programming operation in said logical area taking place in an area of the blank mirror area *(flash memory system which "allows data to be continuously written to unwritten physical address locations," abstract; data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29) (page 7, lines 1 - page 9, line 22 and page 13, claim 1).*

However, Ban does not disclose the flash memory module being on a card.

Robinson discloses a card comprising an electronic module having information process means and a flash type non volatile memory *(abstract; title).*

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a card in the system of Ban, because Robinson teaches it as a way of encasing flash memory and logic circuitry to perform operations of storing and outputting data *(abstract)*.

29. **Claims 14-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** in view of **Hazen et al. (WO 99/35650 hereinafter "Hazen")** as applied to **claims 5 and 6** above, and further in view of **Assar et al. (WO 95/10083 hereinafter "Assar")**.

Consider **claims 14 and 15**, and as applied to **claims 5 and 6** above, Ban in view of Hazen discloses the method comprising designating said active physical areas *(active unit made up of active blocks, FIG. 7; page 9, lines 27-30; page 10, line 1)*.

However, Ban in view of Hazen does not disclose the method comprising designating said active physical areas using a counter incremented on each change of active area.

Assar discloses a method comprising designating active physical areas using a counter *(counter 620 page 18, lines26-page 19, line 1; page 20, line 17 and 26; counter 620 is used in conjunction with flags such as the used/free flag 112)* incremented on each change of active area *(page 20, lines 10-19)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to designate active physical areas using a

counter in the system of Ban in view of Hazen, because Assar teaches a counter is used to show the number of times a block has been erased and written (which areas are most and least worn out) in order to determine where to write next *(page 18, lines 26-28; abstract)*.

Consider **claims 16 and 17**, and as applied to **claims 5 and 6** above, Ban in view of Hazen discloses the method of claims 5 and 6.

However, Ban in view of Hazen does not disclose the method comprising associating at least one bit with a logical area representing the use state of at least one mirror physical area of said logical area.

Assar discloses a method comprising associating at least one bit *(one bit used flag 626, page 18, line 36)* with a logical area *(data block, page 18, lines 31-37)* representing the use state of at least one mirror physical area of said logical area *(page 18, lines 35-37)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate at least one bit with a logical area representing the use state of at least one mirror physical area of said logical area in the system of Ban in view of Hazen, because Assar teaches used/free flag is used to avoid an erase-before-write cycle and therefore avoid the overhead of an erase cycle *(page 7, lines 9-21)*.

30. **Claims 19-20, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** in view of **Hazen et al. (WO 99/35650 hereinafter "Hazen")** as applied to **claim 5 and 6** above, and further in view of **Kuo (US Patent # 4763305 hereinafter "Kuo")**.

Consider **claims 19 and 20**, and as applied to **claims 5 and 6** above, Ban in view of Hazen discloses wherein the write is carried out as claims 5 and 6 above.

However, Ban in view of Hazen does not disclose the method, wherein the write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank physical area otherwise.

Kuo discloses a method, wherein a write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area *(if data in the area is the same as the data to be written, then avoid the erase/program cycle the data and the write is complete for that area, column 6, lines 18-26)*, and in a blank physical area otherwise *(if old data in byte or block is already in erased state or blank, or the data does not match so the physical area is erased or blank and then the write is performed; column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include when the write is carried out in an active physical area if the content of the logical area is identical to the content

of the active physical area or when said write involves no erasure, and in a blank physical area otherwise, in the system of Ban in view of Hazen, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

Consider **claim 22**, and as applied to **claim 19** above, Ban in view of Hazen discloses the method comprising programming *(writing)* of the logical area in the blank physical area in claim 1.

However, Ban in view of Hazen does not disclose the method comprising programming only part of the logical area in the blank physical area.

Kuo discloses a method comprising programming only part of the logical area in the blank physical area *(only erase/program those areas which need to be, those areas that new data is same as old do not need to be erased and subsequently reprogrammed, column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to be able to program only part of the logical area in the blank physical area in the system of Ban in view of Hazen, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

31. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** in view of **Assar et al. (WO 95/10083 hereinafter**

"Assar") as applied to **claim 7** above, and further in view of **Kuo (US Patent # 4763305 hereinafter "Kuo").**

Consider **claim 21**, and as applied to **claim 7** above, Ban in view of Assar discloses wherein the write is carried out as claim 7 above.

However, Ban in view of Assar does not disclose the method, wherein the write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank physical area otherwise.

Kuo discloses a method, wherein a write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area *(if data in the area is the same as the data to be written, then avoid the erase/program cycle the data and the write is complete for that area, column 6, lines 18-26)*, and in a blank physical area otherwise *(if old data in byte or block is already in erased state or blank, or the data does not match so the physical area is erased or blank and then the write is performed; column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include when the write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank physical area otherwise, in the system of Ban in view of Assar, because Kuo

teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew R. Chrzanowski whose telephone number is (571) 270-1176. The examiner can normally be reached on M-Th 7:30am-5:00pm, every other Friday 7:30am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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01/22/07

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